APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/753,259	12/29/2000	Louis A. Lippincott	42390P9946	8787

8791   7590   08/25/2003

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
LOS ANGELES, CA   90025

EXAMINER
SINGH, DALIP K

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 08/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/753,259	LIPPINCOTT, LOUIS A.
	Examiner	Art Unit
	Dalip K Singh	2676

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _09 June 2003_ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-30_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-30_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)   4)☐ Interview Summary (PTO-413) Paper No(s). _____ .

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)   5)☐ Notice of Informal Patent Application (PTO-152)

3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .   6)☐ Other: .

DETAILED ACTION

Response to Amendment

1.   This Office Action is in response to applicant's amendment dated June 9, 2003 in

response to PTO Office Action dated April 9, 2003. The amendments to claim(s) 1, 2, 4, 6, 9, 10,

12, 15-17, and 21-23; and the addition of claim(s) 26-30 have been noted and entered in the

record, and applicant's remarks have been carefully considered resulting in the action as set

forth herein below.

2.   Applicant's arguments filed June 9, 2003 have been fully considered but they are not

persuasive.

3.   Regarding applicant's argument that "Priem 1 may configure memory in such a way that

data may only be scanned from a designated frame buffer; that the a portion of the array 42,

which is never scanned to the display and thus **does not teach or suggest** the controller as

recited in the instant claim 1", applicant's attention is drawn to Priem 1 reference which states

"... on the other hand, once new data has been written to the first (invisible frame buffer) portion

43 of the array 42, the data therein may be transferred to the second (visible frame buffer)

portion 44 from which information may be scanned to the display. This copying from one buffer

to the other is accomplished by the fast copy method...(col. 11, lines 22-45)". Specifically with

respect to claim 1, Priem 1 reference **discloses** a controller (control circuits 40 and 41 in Fig. 3)

to copy identified updated data within the first frame buffer (new data written to the first

portion 43; col. 11, lines 22-23) to the second frame buffer (the data therein may be transferred

to the second portion 44; col. 11, lines 24-25) and a display monitor when the identified data is

needed to refresh the display monitor (from which information may be scanned to the display;

col. 11, lines 25-26). Since Priem 1 discloses new data written to the first portion 43 (invisible

frame buffer), it is inherent that there was an "updated data" within a first frame buffer, such

"updated data" from the first frame buffer is written to or copied to the second frame buffer to

be written to the display monitor under the coordination of control circuits 40 and 41 which

together perform as the controller of the instant claim 1 recitation (emphasis added). Therefore,

claim 1 rejection under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,742,788 to

Priem et al. (Priem 1) is indeed proper. Regarding applicant's argument that "Priem1, as well as

Priem2 strictly prohibit the simultaneous scanning of data from both frame buffers to the

display", applicant's attention is drawn to the similar operations as described above. Regarding

applicant's argument that "Priem1-Hsu combination teaches away from providing a first

memory as part of a unified memory architecture", Priem1 is deficient of unified memory

architecture but does teach single buffer as well as double buffer configuration (mode DBMN

col. 11, lines 1-45). Hsu **discloses** double buffers in frame buffer memory 304b and expansion

frame buffer memory 306 and unified memory architecture. Therefore, it would have been

obvious to a person of ordinary skill in the art the time invention was made to modify Priem1

with the feature "double frame buffers implemented as part of a unified memory architecture" as

taught by Hsu because it provides for a lower system cost.

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2.   Claims 1, 2, 10, 16, 22 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by

U.S. Patent No. 5,742,788 to Priem et al.

      a.   Regarding claim 1, Priem et al. **discloses** a dual frame buffer system (Figure 3),

comprising: a first frame buffer (first frame buffer 43); a second frame buffer (second

frame buffer 44); and a controller (control circuits 40 and 41) for copying identified data

(...once new data has been written to the first portion 43...col. 11, lines 22-25) from the first frame buffer (first frame buffer 43) to the second frame buffer (second frame buffer 44) when identified data is needed to refresh the display monitor (col. 11, lines 1-45).

b.   Regarding claim 2, Priem et al. **discloses** wherein the controller (control circuits 40 and 41) coordinates refresh of the display monitor using data stored in the second frame buffer (second frame buffer 44) and data updated (...once new data has been written to the first...col. 11, lines 23-24) within the first frame buffer (first (invisible frame buffer) portion 43) (...the control circuits cause data to be copied...read from the first frame buffer...and written to the second frame buffer...simultaneously...col. 11, lines 22-45).

c.   Regarding claims 10, it is similar in scope to claim 2 above and is rejected under the same rationale.

d.   Regarding claims 16 and 22, they are similar in scope to claim 10 above and are rejected under the same rationale.

e.   Regarding claim 26, it is similar in scope to claim 1 above and is rejected under the same rationale.

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.   Claims 3, 11 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,742,788 to Priem et al. (Priem1) as applied to claim 1 above, and further in view of

U.S. Patent No. 5,724,608 to Tohara, and further in view of U.S. Patent No. 5,543,824 to Priem

et al (Priem2).

      a.   Regarding claims 3 and 11, Priem1 et al. **does not disclose** the dual frame

buffer system, further comprising: a first address generator corresponding to the first

frame buffer; a second address generator corresponding to the second frame buffer.

Tohara **discloses** a first address generator (1st addresss generator 5) corresponding to

the first frame buffer (1st buffer 12); a second address generator (2nd address generator

5A) corresponding to the second frame buffer (2nd buffer) (Figure 5, col. 5, lines 66-67;

col. 6, lines 1-21). Priem1 and Tohara **do not disclose** a timing generator for

coordinating the timing between the first and second address generators for refreshing

the display monitor. Priem2 **discloses** a timing generator (video timing generator 22)

for coordinating the timing between the first and second address generators for

refreshing the display monitor (col. 4, lines 30-45). Therefore, it would have been

obvious to a person of ordinary skill in the art at the time invention was made to modify

the device as taught by Priem1 with the feature "address generators" as taught by Tohara

and the feature "timing generator" as taught by Priem2 because address generators

provides for a simple processing system design (col. 6, lines 16-17, Tohara) and the

timing generator frees up the central processing system for other tasks (col. 4, lines 15-

45).

      b.   Regarding claim 27, it is similar in scope to claim 11 above and is rejected under

the same rationale.

5.   Claims 4-6, 12-15, 17-19, 21, 23-25, 28, 29 and 30 are rejected under 35 U.S.C. 103(a) as

being unpatentable over U.S. Patent No. 5,742,788 to Priem et al. (Priem1) as applied to claim 1

above, and further in view of U.S. Patent No. 5,724,608 to Tohara, and further in view of U.S.

Patent No. 5,543,824 to Priem et al (Priem2) as applied to claim 3 above, and further in view of

U.S. Patent No. 5,757,364 to Ozawa et al.

     a.   Regarding claims 4 and 12, Priem1-Tohara-Priem2 combination **does not**

disclose a detector for detecting when an update is made to the data in the first frame

buffer; and a decoder for decoding the location of the updated data, wherein the

controller simultaneously transmits the updated data from the first frame buffer to the

second frame buffer and the display monitor when the display monitor is refreshed.

Ozawa et al. **discloses** a detector (window type table 132, comparator 118) for detecting

when an update is made to the data in the first frame buffer; and a decoder (selector 121)

for decoding the location of the updated data (col. 4, lines 36-48; col. 5, lines 1-67; col. 6,

lines 1-41). Therefore, it would have been obvious to a person of ordinary skill in the art

at the time invention was made to modify Priem1-..Priem2 combination with the feature

"detector and decoding and transmitting only the updated data" as taught by Ozawa et al.

because it provides for efficiently rendering frames by transmitting only the updated

data and provides for efficient real time displaying dynamic images (col. 1, lines 40-67).

     b.   Regarding claims 5 and 13, Priem2 et al. **discloses** wherein the first frame buffer

comprises a plurality of regions (contiguous memory 42...is constructed of VRAM...col. 7,

lines 47-67; col. 8, lines 1-7).

     c.   Regarding claims 6 and 14, they are similar in scope to claim 4 above and are

rejected under the same rationale.

     d.   Regarding claims 15, 17, 21 and 23, they are similar in scope to claim 12 above

and are rejected under the same rationale.

     e.   Regarding claims 18, 24 and 28, they are similar in scope to claim 13 above and

are rejected under the same rationale.

f.   Regarding claims 19 and 25, they are similar in scope to claim 14 above and are rejected under the same rationale.

g.   Regarding claim 29, it is similar in scope to claim 4 above and is rejected under the same rationale.

h.   Regarding claim 30, it is similar in scope to claim 6 above and is rejected under the same rationale.

6.   Claims 7-9 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,742,788 to Priem et al. (Priem1) as applied to claim 1 above, and further in view of U.S. Patent No. 5,790,138 to Hsu.

a.   Regarding claims 7 and 9, Priem1 **does not disclose** wherein the first frame buffer is part of a unified memory architecture. Hsu **discloses** a computer unified memory architecture system wherein the first frame buffer (frame buffer memory 304b) is part of a unified memory architecture (col. 3, lines 65-67; col. 4, lines 1-9). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Priem1 with the feature "frame buffer as part of a unified memory architecture" because it provides for a lower system cost (col. 1, lines 62-65).

b.   Regarding claim 8, Hsu **discloses** wherein the second frame buffer (expansion frame buffer memory 306) stores data used to refresh the display monitor (col. 3, lines 65-67; col. 4, lines 1-9).

c.   Regarding claim 20, it is similar in scope to claim 9 above and is rejected under the same rationale.

Conclusion

7.   Applicant's arguments have been fully considered but they are not persuasive.

Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is

reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to **Dalip K. Singh** whose telephone number is **(703) 305-3895.**

The examiner can normally be reached on Mon-Thu (8:00AM-6: 30PM) Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, **Matthew Bella**, can be reached at **(703) 308-6829.**

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,

Arlington, VA, Sixth Floor (Receptionist). Any inquiry of a general nature or relating to the

status of this application or proceeding should be directed to the Technology Center 2600

Customer Service Office at telephone number :(703)-306-0377.

dks

August 20, 2003

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600